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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/788,899

02/27/2004

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EXAMINER

ALANKO, ANITA KAREN

ART UNIT

PAPER NUMBER

1765

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DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/788,899

Applicant(s)

TOREK ET AL.

Examiner

Anita K. Alanko

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/6/07 RCE.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 8-50 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 8-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/6/07</u> . | 6) <input type="checkbox"/> Other: _____ |

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/11/06 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 46-50 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lee et al (KR 2001-037699 A).

Lee discloses a process comprising:

forming a recess in a substrate 120,100 (abstract, lines 11-13, the dry etch step);

forming a conductive structure 130 in the recess having vertical sidewalls (the figures depict vertical sidewalls), wherein the conductive structure is partially embedded in the recess and is formed to extend from the first dielectric stack (see figures); and

electrically isolating the conductive structure (the etch-back step, abstract, line 15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (KR 2001-037699 A) in view of Choi (US 6,080,594) and O'Brien (US 5,817,182)

As to claim 1, Lee discloses a process comprising:

forming a first recess in a substrate 120,100 (abstract, lines 11-13, the dry etch step);

forming a conductive structure 130 in the first recess having vertical sidewalls (the figures depict vertical sidewalls);

first etching ("etch-back process" or SOG elimination, abstract, lines 15-16) to expose a first portion of the conductive structure;

second non-wet etching (dry etch, abstract, lines 16-18) to expose a second portion of the conductive structure, wherein the exposed first and second portions of the conductive structure extend vertically above the substrate 100 (as shown in the figures, note that as broadly interpreted they extend above the substrate since they are formed above the substrate 100, for example they don't extend below the substrate).

Lee fails to disclose (in the abstract) how the etch-back is performed, or how the SOG is eliminated.

Choi teaches that SOG can be eliminated by using wet etching (col.8, lines 24-27). It would have been obvious to one with ordinary skill in the art to use a first wet etching process to

expose a first portion of the conductive structure in the method of Lee because Choi teaches that this is a useful technique for eliminating SOG.

Lee fails to teach first rinsing of the conductive structure.

O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability (col.4, lines 8-13). It would have been obvious to rinse after exposing the conductive structure in the modified method of Lee because O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability.

As to claim 2, Lee discloses etching the a polysilicon sacrificial second film that is disposed over the substrate (the etch-back to expose the 4th oxide).

As to claim 3, Lee and Choi do not disclose the etch rates. However, the etch rate is result effective variable since a fast etch rate saves time whereas a slow etch rate provides for more control. It would have been obvious to one with ordinary skill in the art to etch at the cited rates in the modified method of Lee because the etch rate appears to reflect a result-effective variable which can be optimized. See MPEP 2144.05 IIB.

As to claim 4, Choi teaches that the first etching includes a wet process (SOG removal) and Lee discloses that the second etching is a dry process (dry etch).

As to claim 5, Lee teaches that the substrate includes a single dielectric stack 110,120, however the abstract does not disclose how they are deposited. It would have been obvious to one with ordinary skill in the art to form by vapor deposition since it is a conventional technique for forming dielectric layers.

Claims 6, 8-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (KR 2001-037699 A) in view of Choi (US 6,080,594), O'Brien (US 5,817,182) and Kang et al (US 2004/0175884 A1).

The discussion of modified Lee from above is repeated here.

As to claim 6, Lee does not disclose the composition of an oxide. Kang teaches that a useful composition for forming capacitors similar to Lee is phospho silicate glass 220 ([0037]). It would have been obvious to one with ordinary skill in the art to form PSG as the oxide in the modified method of Lee because Kang teaches that it is a useful composition for forming oxides in methods to form capacitors.

As to claims 8-9, the modified method of Lee discloses to form the recess in a dielectric first film 110 that is disposed above the substrate 10, and that oxide 120 of Lee is useful to form, as taught by Kang, to be PSG sacrificial second film 220 (since it is removed in Fig.3G). It would have been obvious to one with ordinary skill in the art that the second film (PSG in the modified method of Lee) is a sacrificial film because Kang teaches that it is useful to form the final product without the oxide film.

As to claim 10, it would have been obvious to include polysilicon, as broadly cited, since it is a conventional film in a multi-level semiconductor device.

As to claims 11-21, see the rejection of claims 1 and 5.

Claims 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (KR 2001-037699 A) in view of Jost et al (US 5,966,611) and Sell (US 2004/0147074 A1).

The discussion of Lee from above is repeated here.

As to claim 40, Lee discloses a process comprising:

stripping a material (SOG) from a conductive structure 130 (polysilicon) embedded therein having vertical sidewalls (see figures), wherein the conductive structure is coupled to a substrate active area 100.

Lee fails to teach that the material that is stripped is amorphous carbon.

Jost teaches that a sacrificial film 54 over a conductive structure 50 (Fig.4) may comprise silicon oxide or amorphous carbon (col.3, lines 43-48). Jost also teaches that the amorphous carbon may be selectively etched from polysilicon (col.4, lines 61-62). It would have been obvious to one with ordinary skill in the art to selectively etch amorphous carbon from the conductive structure in the method of Lee because Jost teaches that it is a useful, alternative material for silicon oxide in methods to form capacitors.

Lee fails to explicitly disclose the aspect ratio. The aspect ratio determines the density and properties of the final device device, in that a higher aspect ratio.

Sell teaches that trench capacitors typically have aspect ratios within the range cited ([0020]). It would have been obvious to vary the aspect ratio to that cited because Sell teaches that they are a useful, typical value for trench capacitors.

As to claim 41, Lee discloses that the conductive structure includes a container capacitor and Jost teaches that the amorphous carbon may be striped by an oxygen plasma (col.4, lines 61-63).

As to claims 42-45, it would have been obvious to include a TEOS-silicon oxide, BPSG, or polysilicon a broadly cited, since they are conventional films in semiconductor devices.

Claims 22-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,764,947 B1) in view of O'Brien (US 5,817,182).

As to claim 22, Chan discloses a process comprising:

first etching a sacrificial second film 26 (Fig.3b-3c) to expose a first portion (the portion defined by the undercut) of a conductive structure 18, wherein first etching includes a first etch chemistry and wherein first etching includes a first etch rate; and

second etching an amorphous carbon first film 22 to expose a second portion of the conductive structure 18 (as shown in Fig.3b), wherein second etching includes a second etch chemistry.

Chan fails to explicitly disclose rinsing the conductive structure. Chan teaches that cleaning may be used, as is apparent to those having ordinary skill in the art (col.4, lines 47-57). O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability (col.4, lines 8-13). It would have been obvious to rinse the conductive structure in the method of Chan because O'Brien teaches that it is useful to rinse after etching in order to remove etchant residues that may impact subsequent processing, device yield or reliability.

As to claims 22, 23 and 29, Chan also fails to disclose the relative etch rates of the first etch rate and second etch rate. However, the etch rate is result effective variable since a fast etch rate saves time whereas a slow etch rate provides for more control. It would have been obvious to one with ordinary skill in the art to etch at the cited rates in the modified method of Chan because the etch rate appears to reflect a result-effective variable which can be optimized. See MPEP 2144.05 IIB.

As to claims 24-28, 30-39, Chan discloses that the sacrificial second film is a silicon oxide that may be formed “in a variety of manners” such as vapor deposition (col.3, lines 17-20). Chan fails to disclose whether the silicon oxide is doped or undoped. O’Brien teaches some useful silicon oxides such as doped and undoped (BPSG, TEOS col.1, line 50), which are obvious to spin-on process or vapor deposit since they are conventional processing techniques in the art. It is also conventional to dope polysilicon as desired to achieve the desired level of conductivity.

Response to Amendment

The claims remain rejected over Lee and Chan.

Response to Arguments

Applicant's arguments filed 12/11/06 have been fully considered but they are not persuasive.

Applicant, on page 10 in the “Remarks” section argues about perpendicular and equivalents. Examiner does not understand how a tapered wall is also perpendicular since perpendicular has a clear meaning. However, if applicant considers tapered walls to read on perpendicular then a full response will include amendments to overcome the previous rejections in previous office actions over Kang.

In the arguments on page 10 in “Information Disclosure Statement” section, applicant argues that applicant has not reviewed the documents that have not been considered by examiner.

In response, they have been crossed out from the IDS statement because they are not related to the instant invention. Applicant is invited to submit a statement as to how they are related.

The remaining arguments focus on vertical sidewalls extending above the substrate. In response, the sidewalls extend above the substrate because they are above the substrate. Examiner acknowledges that Lee is different from what is depicted in the figures of the instant invention, however the claims are of a broad scope and Lee reads on the claimed invention. For example, the claims do not cite that the first and second portions are etched and thereby released from all of the surrounding substrate material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K. Alanko whose telephone number is 571-272-1458. The examiner can normally be reached on Mon-Fri until 2:30 pm (Wed until 11:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit: 1765

Anita K. Alanko

Anita K Alanko
Primary Examiner
Art Unit 1765